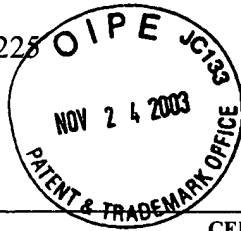


Appl. No.: 10/644,225

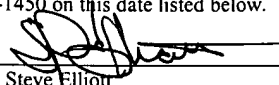


Patent
Docket No. CA7017522001

CERTIFICATE OF MAILING

I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this date listed below.

Dated: November 19, 2003

Name of Person Certifying: 

Printed Name: Steve Elliott

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/644,225

Applicant: Igor Keller

Filing Date: August 19, 2003

Title: RECEIVER DEPENDENT SELECTION OF A WORST-CASE TIMING
EVENT FOR STATIC TIMING ANALYSIS

Examiner: Unknown

Group Art Unit: Unknown

Docket No.: CA7017522001

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. § 1.56, the references listed on the attached forms PTO-1449a and PTO-1449b are being brought to the attention of the Examiner for consideration in connection with the examination of the above-identified patent application. The Examiner is requested to make these documents of record.

I. Timing of the Information Disclosure Statement:

This Information Disclosure Statement is filed:

- ☒ Within three months after the filing date of the application or within three months after the date of entry of the national stage of a PCT application as set forth in 37 C.F.R. § 1.491.

II. Copies of the Cited Items:

☒ Copies of all of the items listed on the attached Form PTO/SB/08A are enclosed.

III. Concise Explanation of Relevance:

☒ A concise explanation of relevance of the items listed on Form PTO/SB/08A is not given.

IV. Conclusion:

Citation of the above documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

It is respectfully requested that the Examiner indicate consideration of the cited references by returning a copy of the attached form PTO 1449 with initials or other appropriate marks. The Commissioner is hereby authorized to charge Deposit Account No. 50-2518, billing reference number: CA7017522001 for any additional fees required in connection with the filing of this Information Disclosure Statement.

DATE: November 19, 2003

Respectfully submitted,

By: Jeffrey S. Smith
Jeffrey S. Smith
Registration No. 39,377

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A-PTO

Complete if Known

Application Number	10/644,225
Filing Date	August 19, 2003
First Named Inventor	Igor Keller
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket No.	CA7017522001



INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Use as many sheets as necessary)

1 of 1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number Number – Kind Code ² (if known)	Publication Date MM-DD-YY	Name of Patentee or Application of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ – Number ⁴ – Kind Code ⁵ (if known)	Publication Date MM-DD-YY	Name of Patentee or Application of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
		L. McMurchie and C. Sechen. WTA – Waveform-Based Timing Analysis for Deep Submicron Circuits. In <i>Proc. IEEE/ACM International Conference on Computer-Aided Design, 2002</i>	
		N.H.E. Weste and K. Eshraghian, "Principles of CMOS VLSI Design," 2 nd edition, pages 442-446, 469-471, 645-653, Addison-Wesley Publishing Company 1993	
		J. Qian, S. Pullela, and L.T. Pillage, "Modeling the 'Effective Capacitance' for the RC Interconnect of CMOS Gates," <i>IEEE Transactions on CAD, vol. 13, No. 12, pp. 1526-1535.</i>	

Examiner's
SignatureDate
Considered

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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